REMARKS

This paper is in response to the Office Action mailed June 1, 2006. Claims 1, 3-6, 8-11, 13-16, and 18-24 are pending. The specification has been amended to correct typographic errors. No new matter is added. Reconsideration of this application is respectfully requested in view of this response.

Claims 1, 3-6, 8-11, 13-16 and 18-24 are rejected under U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,873,003 to Inoue et al. (hereinafter referred to as Inoue) in view of the Applicant's Allegedly Admitted Prior Art (hereinafter referred to as AAAPA). Applicants respectfully traverse.

To be properly rejected under 35 U.S.C. §103(a), the cited reference(s) must teach each and every limitation of the rejected claims. Applicant respectfully contends that Inoue fails to teach or render obvious many of the features of Applicant's pending claims.

Inoue teaches a liquid crystal display unit for a view finder having a sight line detecting function comprising a pair of substrates, a liquid crystal material sealed between said pair of substrates, semiconductor elements provided at either substrate for driving the liquid crystal display unit, and photoelectric conversion elements provided at either substrate, for detecting the sight line.

With respect to claims 1 and 11, the Examiner on page 3 of the Office Action of June 1, 2006, contends that Inoue, on column 19, lines 8-15, teaches a source driver circuit having "a resetting means for resetting the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set". However, the cited section of Inoue is reproduced below:

> A ***reset voltage is applied during the blanking period*** so that the drain region 1305 and the semiconductor region 1308 having opposite conduction type to that of drain region are first placed in reverse bias state. Then, the switching TFT is turned off to place the drain region in an electrically floating state.

(Inoue; col. 19, lines 8-15; emphasis added). There is no disclosure or suggestion that the reset voltage in Inoue is applied in a blanking period of ***each*** of the horizontal synchronizing periods of the set, as recited in the claim. The Examiner's citation of column 19 is a continuation of Inoue's discussion of "Embodiment 12" starting at column 17, lines 32 et seq. In embodiment 12, Inoue apparently discusses a method for driving a LCD unit whereby there is no necessity of disposing the sight line detecting sensor separately and there is no necessity for providing a new driving circuit for the sight line sensor.

However, lacking in the above-citation and the entire description of Inoue is a teaching for the features of "a polarity of a data applied to each the pixels ...is *inverted in every set of two or more horizontal synchronizing periods*" and a "resetting means for resetting the data voltages outputted by the source driver circuit in *a blanking period of each of the horizontal synchronizing periods of the set*" (emphasis added) – features of claims 1 and 11.

The Examiner is respectfully referred to Figure 7 (which is reproduced below for the convenience of the Examiner) of the application-as-filed with regards to the importance of resetting the data voltages in a blanking period of *each* of the horizontal synchronizing periods.

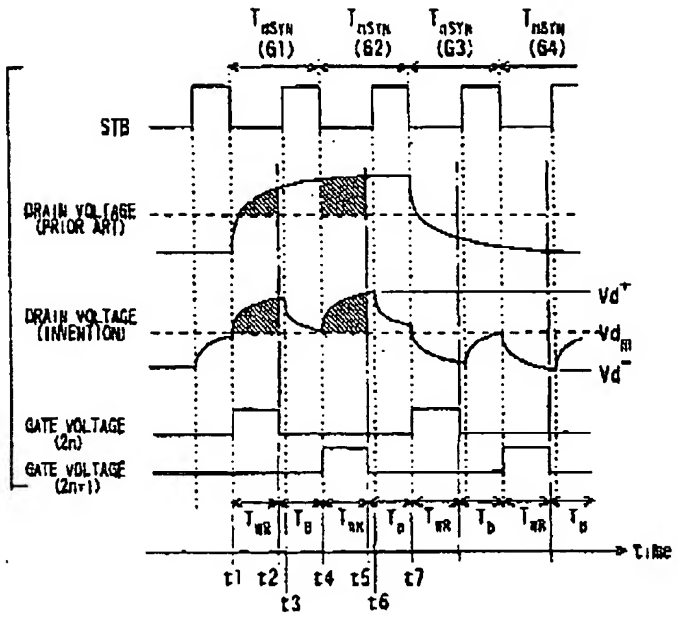


FIGURE 7 OF APPLICATION-AS-FILED

As can be seen from the figure above, a problem with the prior art (shown as the graph of the "Drain Voltage (Prior Art)") is that the amount of charge written into the respective pixels connected to the first gate line G1 is likely to be less than that written into the respective pixels connected to the second gate line G2 (note the difference in the shaded areas), thereby generating luminance difference between the first and second gate lines G1 and G2.

Claims 1 and 11 solve this problem by teaching the resetting of data voltages in a blanking period of *each* of the horizontal synchronizing periods. In the first horizontal synchronizing periods T_{HSYN}, the output of the shift register/latch circuit is reset at the time t2 prior to the time t3. The resetting circuit is controlled in such a way that each of the data voltages will reach a middle point value between a positive peak value and a negative peak value after the resetting operation is completed. Therefore, the data voltage applied to each of the

corresponding pixels PX by the source driver circuit in *each* of the horizontal synchronizing periods ($=2T_{HSYN}$) is made uniform by the resetting operation. This means that the total amount of the charge written into the pixels PX (i.e., the area of the hatched part in FIG. 7) in the first one of the two horizontal synchronizing periods ($=2T_{HSYN}$) of every polarization inversion period can be equalized to that of the charge written into the pixels PX in the second one of the same horizontal synchronizing periods. Hence, the feature of resetting the data voltages in a blanking period of each of the horizontal synchronizing periods allows for writing the same amount of charge into the respective pixels connected to the first gate line G1 and the respective pixels connected to the second gate line G2 (note similarly shaded areas), thereby avoiding a decrease in luminance.

Hence, Applicant respectfully asserts that Inoue, AAAPA, or the combination of Inoue and AAAPA, the propriety of which is respectfully not conceded, fail to teach the polarity of a data applied to each the pixels being inverted in every set of two or more horizontal synchronizing periods and a resetting means for resetting the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing periods of the set. Absent such a showing, Applicant respectfully asserts that claims 1 and 11 cannot be rendered obvious by the combination of Inoue and AAAPA.

If the Examiner still feels that the combination of Inoue and AAAPA teach the resetting of data voltages in a blanking period of *each* of the horizontal synchronizing periods, Applicant respectfully reminds the examiner that it is the duty of the examiner to specifically point out each and every limitation of a claim being rejected as per §1.104(c)(2) of Title 37 of the Code of Federal Regulations and section 707 of the M.P.E.P., which explicitly states that "the particular

part relied on must be designated" and "the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified".

With respect to claims 6 and 16, the Examiner on page 5 of the Office Action of June 1, 2006, once again relies on Inoue and AAAPA as teaching all the features of the rejected claims. However, the Examiner in the Office Action fails to specifically point out where in Inoue, or where in AAAPA, is a teaching for "a polarity inverting means for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing period of the set" – a feature of claim 6. The Examiner in the Office Action also fails to specifically point out where in Inoue, or where in AAAPA, is a teaching for "inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of each of the horizontal synchronizing periods of the set" – a feature of claim 16.

The Examiner in the Office Action of June 1, 2006, single-handedly relies on the AAAPA for providing such a teaching. However, Applicant respectfully points out that nowhere in the specification has the Applicant acquiesced to having knowledge of a prior art mechanism for inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing period of the set.

The Examiner is respectfully referred to Figure 8 (which is reproduced below for the convenience of the Examiner) of the application-as-filed with regards to the importance of inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing periods.

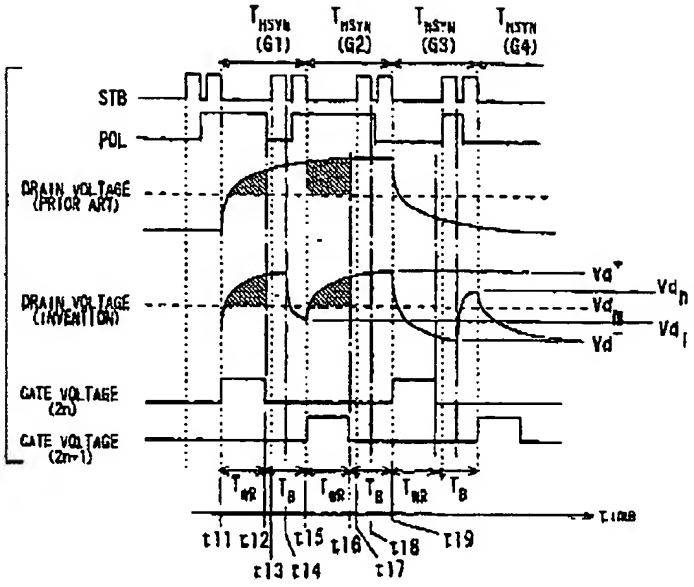


FIGURE 8 OF APPLICATION-AS-FILED

As stated previously and as reinforced in the above-figure, a problem with the prior art (shown as the graph of the "Drain Voltage (Prior Art)") is that the amount of charge written into the respective pixels connected to the first gate line G1 is likely to be less than that written into the respective pixels connected to the second gate line G2 (note the difference in the shaded areas), thereby generating luminance difference between the first and second gate lines G1 and G2.

Claims 6 and 16 solve this problem by inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing period of the set. In the first horizontal synchronizing periods T_{HSYN}, the output of the shift register/latch circuit is polarity-inverted at the time t14 prior to the time t15. Therefore, the value of the data voltage gradually decreases from the positive peak value Vd^+ to a negative voltage

value Vd_l. The polarity inversion operation is carried out in the blanking period T_B. The polarity inverting circuit is controlled in such a way that each of the data voltages will reach the opposite-polarity value Vd_n or Vd_l across the middle point line of Vd_m after the polarity inversion operation is completed. Therefore, the data voltage applied to each of the corresponding pixels PX by the source driver circuit in each of the horizontal synchronizing periods ($=2T_{HSYN}$) is made uniform in the rising state by the polarity inverting operation. This means that the total amount of the charge written into the pixels PX (i.e., the area of the hatched part in FIG. 8) in the first one of the two horizontal synchronizing periods ($=2T_{HSYN}$) of every polarization inversion period can be equalized to that of the charge written into the pixels PX in the second one of the same horizontal synchronizing periods. Hence, the feature of inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing period of the set allows for writing the same amount of charge into the respective pixels connected to the first gate line G1 and the respective pixels connected to the second gate line G2 (note similarly shaded areas), thereby avoiding a decrease in luminance.

Hence, Applicant respectfully asserts that Inoue, AAAPA, or the combination of Inoue and AAAPA fail to teach a means to invert the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing period of the set. Absent such a showing, Applicant respectfully asserts that claims 6 and 16 cannot be rendered obvious by the combination of Inoue and AAAPA.

If the Examiner still feels that the combination of Inoue and AAAPA teach the feature of inverting the polarity of the data voltages outputted by the source driver circuit in a blanking period of *each* of the horizontal synchronizing period of the set, Applicant respectfully reminds the examiner that it is the duty of the examiner to specifically point out each and every limitation

of a claim being rejected as per §1.104(c)(2) of Title 37 of the Code of Federal Regulations and section 707 of the M.P.E.P., which explicitly states that "the particular part relied on must be designated" and "the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified".

The above-mentioned arguments with regards to independent claims 1, 6, 11, and 16 substantially apply to independent claims 21-24 as they recite many similar features.

Based on the arguments presented above, Applicant respectfully requests the Examiner to withdraw the rejections with respect to independent claims 1, 6, 11, 16, and 21-24, and hereby requests allowance thereof. Applicant also respectfully requests the Examiner to withdraw the rejections with regards to dependent claims 3-5, 8-10, 13-15, and 18-20 as they depend from an allowable claim.

SUMMARY

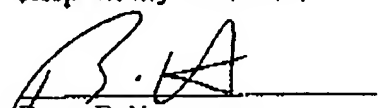
As has been detailed above, none of the references, cited or applied, provide for the specific claimed details of Applicant's presently claimed invention, nor renders them obvious. It is believed that this case is in condition for allowance and reconsideration thereof and early issuance is respectfully requested.

As this response/amendment has been timely filed, no request for extension of time or associated fee is required However, the Commissioner is hereby authorized to charge any deficiencies in the fees provided to Deposit Account No. 50-1290.

Docket: NECA 20.522
Application: 10/625,091

If it is felt that an interview would expedite prosecution of this application, please do not hesitate to contact Applicant's representative at the below number.

Respectfully submitted,



Brian E. Hennessey
Reg. No. 51,271

CUSTOMER NUMBER 026304
Telephone: (212) 940-8800
Fax: (212) 940-8986/8987
575 Madison Avenue
New York, NY 10022-2585